Automotive 160mΩ Dual Channel Fully Protected Automotive Low-side Switch

Datasheet EN

Product Overview

NSD12416-Q1 is a 160mΩ 2 channel low-side switch with 48V clamp voltage for automotive applications. It's designed for driving resistive or inductive loads with one side connected to the battery. Internal 48V clamp circuit protects device from surge energy when fast demagnetization at turn-off.

With internal output current limitation, the device is protected in overload condition. Built-in thermal shutdown protects the chip from over-temperature and short-circuit. A thermal swing mechanism is built to limit dissipated power to decelerate power accumulation. Thermal shutdown, with automatic restart, allows the devices to recover normal operation as soon as a fault condition disappears.

An internal diagnose function is built to indicate any faults when thermal shutdown through an open-drain status output pin. This device operates in ambient temperatures from – 40° C to 125 ° C.

Key Features

- AEC-Q100 (Grade 1) qualified for automotive application
- Drain current limitation: 2.5 A
- 48V overvoltage clamp
- Thermal shutdown protection
- Thermal swing protection
- Fault diagnostic block
  - Thermal shutdown diagnosis
- Very low standby current
- Very low electromagnetic susceptibility
- ESD protection
- RoHS & REACH Compliance

Typical Application

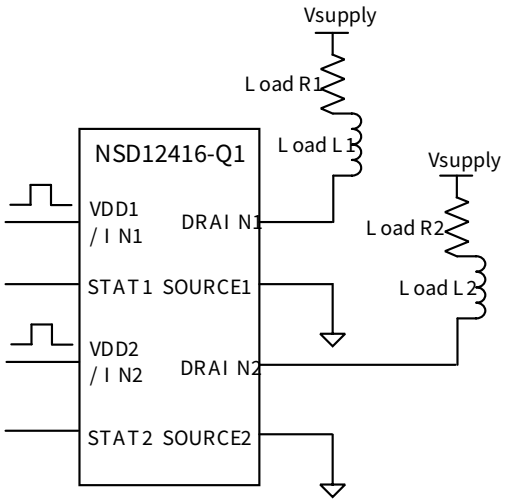

Figure 0.1 NSD12416-Q1 Typical Application

Applications

- Automotive Relays
- Valves
- Solenoid drivers
- Lighting

Device Information

Part Number	Package	Body Size
NSD12416-Q1SPR	SO-8	4.9 mm x 3.9 mm

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Pin Configurations and Functions

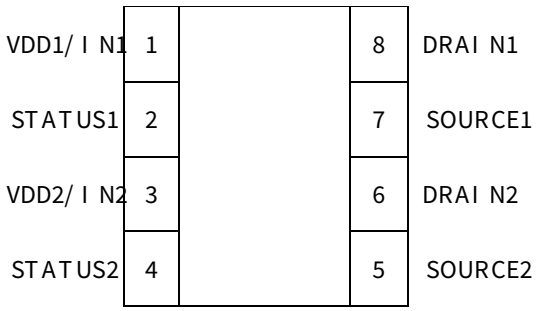
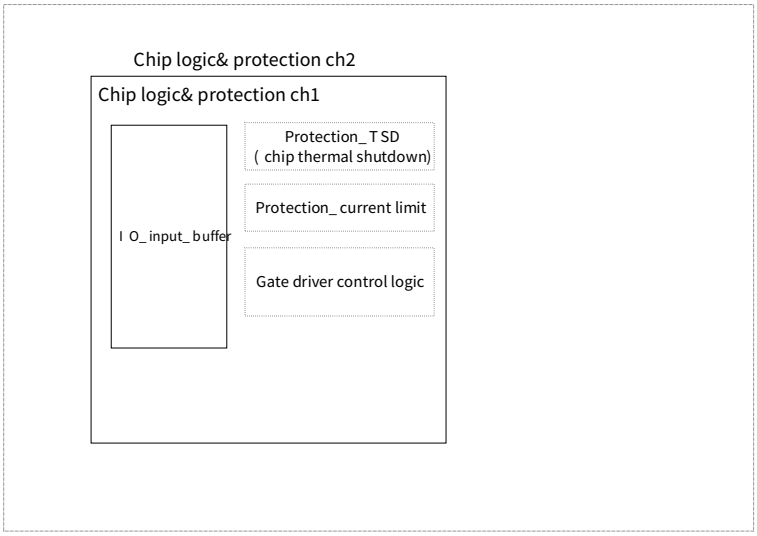


Figure 1.1 NSD12416-Q1SPR Pinout

Table 1.1 NSD12416-Q1SPR Pin Configuration and Description

PIN NO	SYMBOL	FUNCTION
1,3	VDD1,2/IN1,2	Voltage controlled input pin with hysteresis, CMOS compatible. They control output switch state
2,4	STATUS1,2	Open drain digital diagnostic pin
8,6	DRAIN1,2	PowerMOS drain
7,5	SOURCE1,2	PowerMOS source and ground reference for the control section

Block diagram



Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Drain-to-Source Voltage	V_{DS}			Internally clamped	V
DC Drain Current	I_D			Thermal limited	A
INPUT Pin Current	I_{VDD}	-1		10	mA
STATUS Pin Current	I_{STAT}	-1		10	mA
Junction Temperature	T_J	-40		150	°C
Storage Temperature	T_{stg}	-55		150	°C
Single pulse avalanche energy (L_J = 12mH; T_J = 150 °C; R_L = 0Ω; I_{OUT} = I_{lim})	E_{AS}			40	mJ

4 ESD Ratings

Parameters	Symbol	Value	Unit
V(ESD) Electrostatic discharge	Human-body model, per AEC-Q100-002-RevD, $V_{ESD-HBM}$	±4000	V
	Charged-device model, per AEC-Q100-011-RevB, $V_{ESD-CDM}$	±750	V

Other Information

Parameters	Symbol	Value	Unit
Junction-to-ambient Thermal Resistance	θ_{JA}	77.8	°C/W
Junction-to-top characterization parameter	ψ_{JT}	4.25	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	25	°C/W

The thermal data is based on the JEDEC standard high-K profile, JESD51-7, four layers board.

Electrical Characteristics

Electrical Characteristics

(V_{DD} = V_{IN} = 4.5 V to 5.5 V, T_J = -40° C to 150° C. Unless otherwise noted.)

Parameters	Symbol	Min	Typ	Max	Unit	Conditions
Power MOSFET						
ON-state resistance	R_{ON}		160		mΩ	I_D = 1 A; T_J = 25° C; V_{DD} = V_{IN} = 5 V
				320	mΩ	I_D = 1 A; T_J = 150° C; V_{DD} = V_{IN} = 5 V
Drain-source clamp voltage	V_{CLAMP}	46	48	56	V	V_{IN} = 0V, I_D = 1A
Drain-source clamp threshold voltage	V_{CLTH}	40			V	V_{IN} = 0V, I_D = 2 mA
OFF-state output current	I_{DSS}	0		3	μA	V_{IN} = 0 V; V_{DS} = 13 V; T_J = 25° C
		0		5	μA	V_{IN} = 0 V; V_{DS} = 13 V; T_J = 125° C
Body diode forward voltage	V_{BD}		0.8		V	I_D = 1A; V_{IN} = 0 V
Input section						
Supply current from input pin	I_{ISS}		30	65	μA	ON-state; V_{DD} = V_{IN} = 5 V; V_{DS} = 0 V
Input clamp voltage	V_{CL}	5.5		8	V	I_{ICL} = 1 mA
			-0.7			I_{ICL} = -1 mA
Input threshold voltage	V_{INTH}	1		3.5	V	V_{DS} = V_{IN}, I_D = 1 mA
Status Indicator						
Status low output voltage	V_{STAT}			0.5	V	I_{STAT} = 1 mA
Status leakage current	I_{LSTAT}			10	μA	V_{STAT} = 5 V
Status pin input capacitance	C_{STAT}			100	pF	V_{STAT} = 5 V
Status clamp voltage	V_{STCL}	5.5		8	V	I_{STAT} = 1 mA
			-0.7			I_{STAT} = - 1 mA
Switching characteristics						
Turn-on delay time	$t_{d(ON)}$		9		μs	R_L = 13 Ω, V_{DS} = 13 V
Turn-off delay time	$t_{d(OFF)}$		9		μs	R_L = 13 Ω, V_{DS} = 13 V
Rise time	t_r		9		μs	R_L = 13 Ω, V_{DS} = 13 V
Fall time	t_f		5		μs	R_L = 13 Ω, V_{DS} = 13 V
Switching energy losses at turn-on	W_{ON}		26		μJ	R_L = 13 Ω, V_{DS} = 13 V
Switching energy losses at turn-off	W_{OFF}		23		μJ	R_L = 13 Ω, V_{DS} = 13 V

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Protection and diagnostics						
DC short-circuit current	I_{lim}	1.6	2.5	3	A	V_{BS} = 13 V, V_{DD} = V_{IN} = 5 V
Shutdown temperature	T_{TSD}	150	175	200	°C	
Reset temperature	T_R	T_{RS} + 1	T_{RS} + 5		°C	
Thermal reset of STATUS	T_{RS}	135			°C	
Thermal hysteresis (T_{SD} - T_R)	T_{HYST}		7		°C	
Dynamic temperature	ΔT_J		40		K	T_J = -40° C, V_{BS} = 13 V
Dynamic temperature hysteresis	$\Delta T_{J(HYS)}$		15		K	

6.2. Typical Performance Characteristics

Table 6.2.1 Truth table

Conditions	Input	Drain	Status
Normal operation	L	H	H
	H	L	H
Current limitation	L	H	H
	H	X	H
Over-temperature limitation	L	H	H
	H	H	L
VDD under-voltage	L	H	X
	H	H	X

Switching characteristics

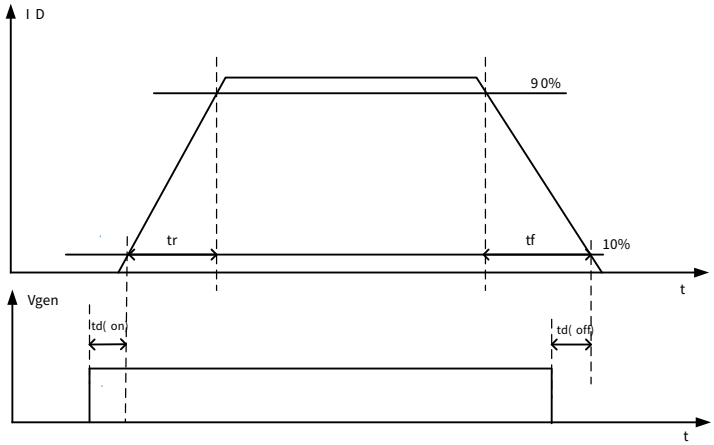


Figure 6.2.2 NSD12416-Q1 Switching Characteristics

Protections

Current Limitation

NSD12416-Q1 has current limitation to protect the silicon and bonding wire in case of overload or short circuit to battery.

Thermal shutdown and thermal swing

This device has both absolute and dynamic temperature protection. There are two thermal sensors on the controller and the MOSFET, the one on the MOSFET is the hottest and the one on the controller is the coldest. The absolute temperature protection is to shut down the MOSFET when the hottest junction temperature exceeds the T_{TSD}, and the dynamic temperature protection is also to shut down the MOSFET when the temperature difference between the hottest and the coldest exceeds ΔT_J.

Application Information

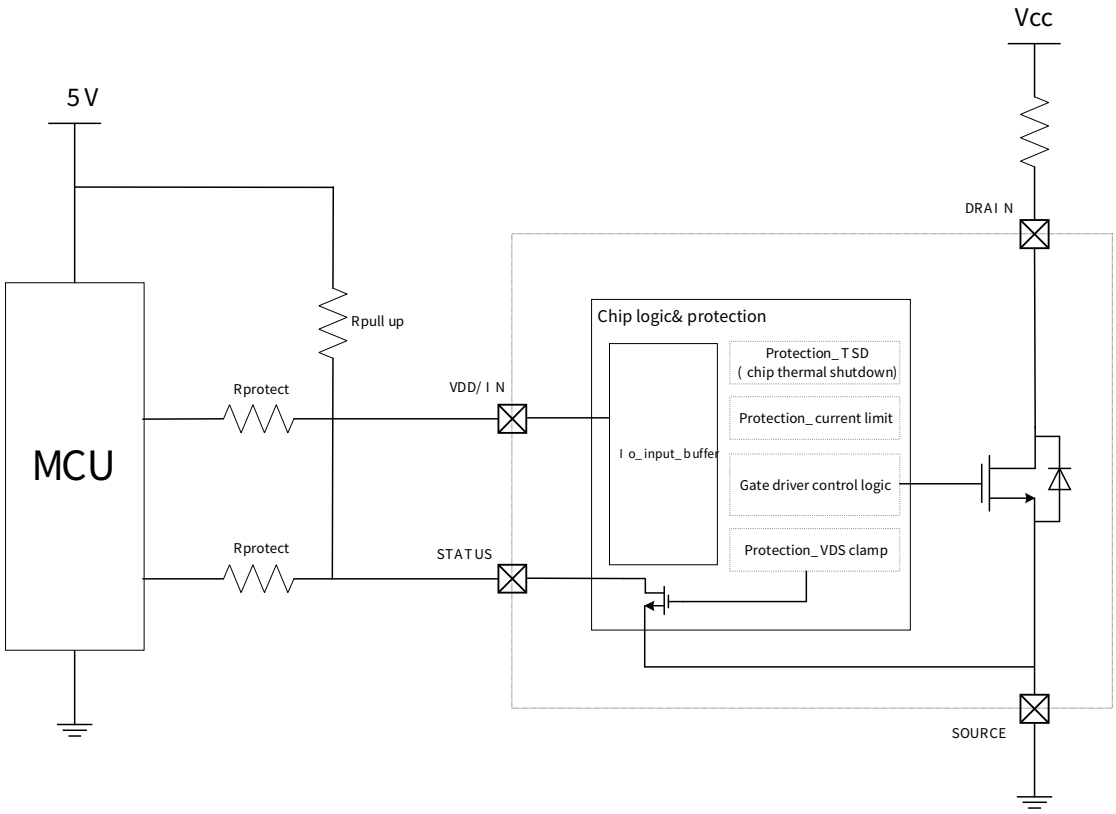


Figure 8.1 NSD12416-Q1SPR application schematic

MCU I/O protection

NSD12416 has Zener diodes inside for ESD protection and the intrinsic NPN parasitic bipolar, so that resistors for protection are necessary in series with the digital inputs to limit the current to protect MCU I/Os during transient and reverse battery conditions.

The value of resistors for protection can be calculated by the formula as shown below:

$$\frac{0.7}{I_{latchup}} \le R_{prot} \le \frac{V_{MCU\_OUT} - V_{IH}}{I_{IHmax}}$$

Where $I_{latchup}$ is the MCU I/O latch up current, V_{MCU_OUT} is the output voltage of MCU I/O, V_{IH} is the High-level input voltage of NSD12416, I_{IH} is the High-level input current.

Let: $I_{latchup} \ge 20mA$; $V_{MCU\_OUT} \ge 4.5V$, so $35\Omega \le R_{prot} \le 15k\Omega$, the recommended value is $1k\Omega$.

The value of [redacted] pull-up resistor

Because the STATUS pin is open drain output, a pull-up resister is needed to fix the high voltage during normal operation. When the fault occurs, the voltage level of STATUS is pulled down by the internal MOSFET on. The value of pull up resistor can be calculated by the formula as shown below:

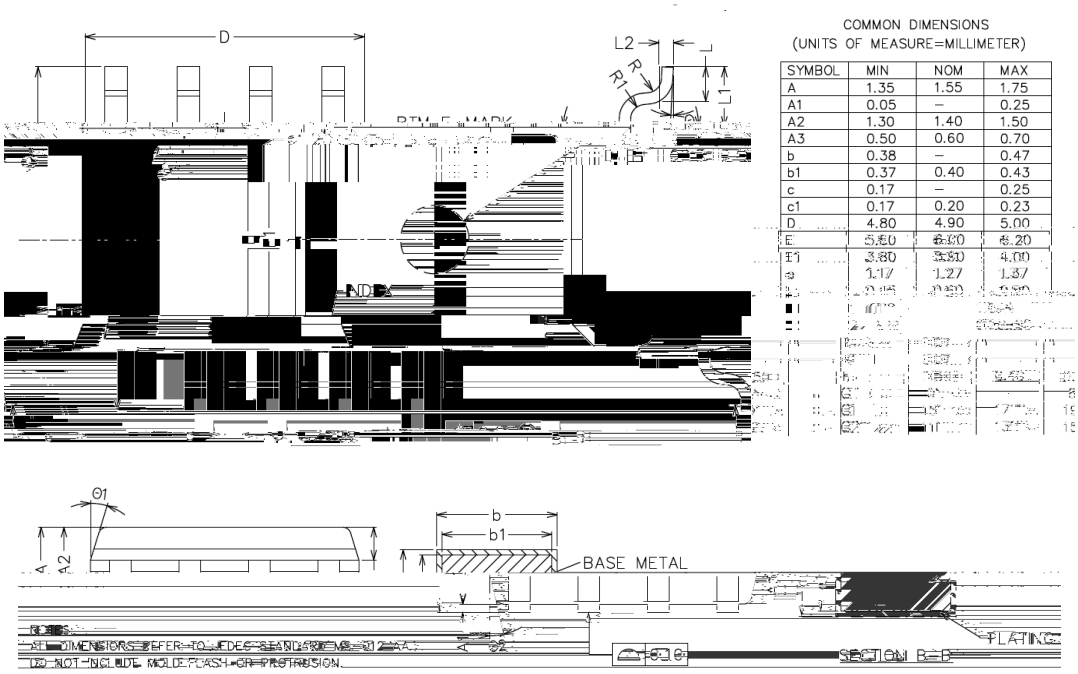
$$\left(\frac{V_{pull\text{-}up}}{V_{OL}} - 1\right) \cdot R_{on} < R_{pull\text{-}up} < \frac{V_{pull\text{-}up} - V_{OH}}{I_{leak}}$$

Where V_{pullup} is the minimum of pull-up supply, V_{OL} is the max imum of MCU logic low, R_{on} is the on resistance of the MOSFET of STATUS pin, V_{OH} is the minimum of MCU logic high, I_{leak} is the max imum leakage current of STATUS pin.

Let: $V_{pullup} = 4.5V$; $Ron = V_{STAT} / I_{STAT} = 500\Omega$, $V_{OL} = 0.9V$, $V_{OH} = 2.1V$, $I_{leak} = 10uA$, so $2k\Omega \le R_{pullup} \le 240k\Omega$.

Package Information

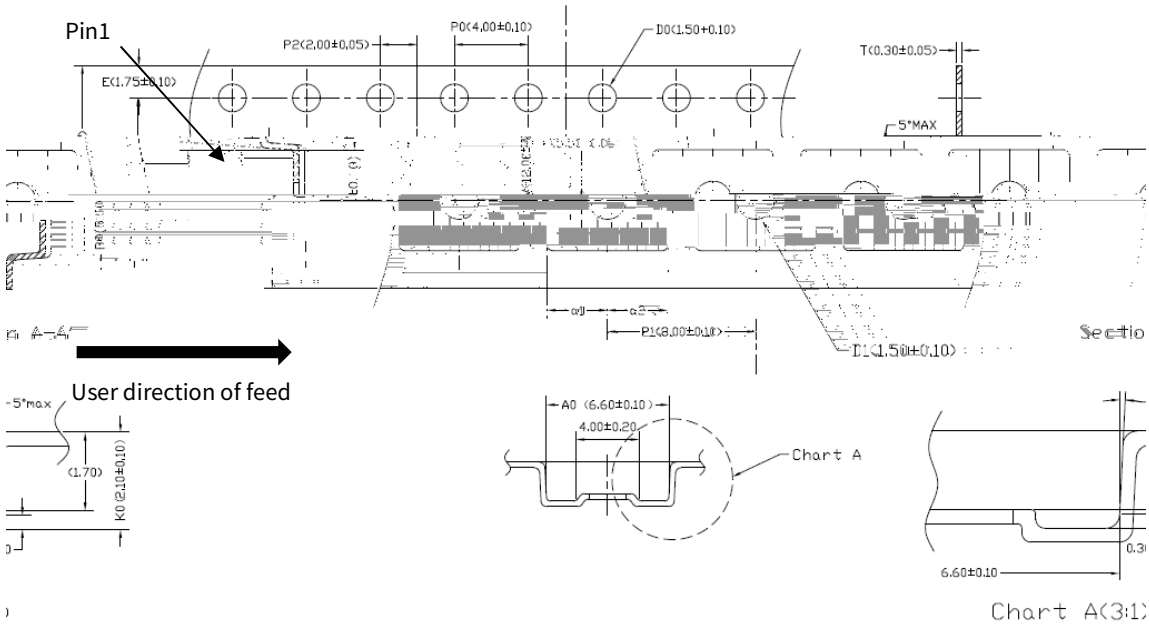
Package information

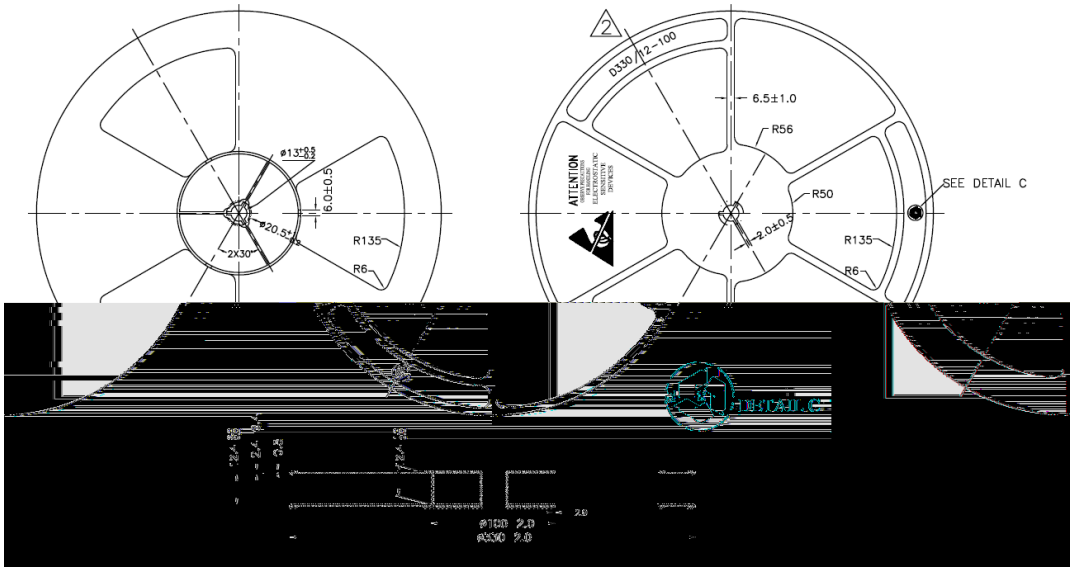


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.05	–	0.25
A2	1.30	1.40	1.50
A3	0.50	0.60	0.70
b	0.38	–	0.47
b1	0.37	0.40	0.43
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.17	1.27	1.37

Packaging information





, Order ng Infor at on

Part Nu ber	Pac age	M[redacted]	[redacted]
NSD12416-Q1SPR	SO-8	3	25 00
Note: A ll pack ages are R OHS compliant with peak re w temperature of 260° C according to the J EDEC ind stry standard classifications and peak solder temperature.			

ev s on H story

ev s on	Descr pt on	Date
1.0	I nitial version	2024/ 2/ 1
1.1	Update k ey description	2024/ 3 / 26
1.2	Update format	2024/ 4/ 7

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