N D Q

CH· Ω· ·Fu ly Protected
Auto ot ve Low s de w tch

Datasheet EN

Product Overv ew

NSD11416-Q1 is a 160mΩ low-side switch with 48V clamp voltage for automotive applications. I t' s designedfor driving resistive or inductive loads with one side connected to the b attery. I nternal 48V clamp circuit protectsdevice from surge energy when fast demagnetiz ation at turn-off.

Wth internal output current limitation, the device is protected in overload condition. Built-in thermal shutdown protects the chip from over-temperature and short-circuit. A thermal swing mechanism is b uilt to limit dissipated power to decelerate power accumulation. T hermal shutdown,with automatic restart, allows the devices to recover normal operation as soon as a fault condition disappears.

An internal diagnose function is b uilt to indicateany faults when thermal shutdown and short circuit to ground conditions through an open-drain status output pin. T his device operates in amb ient temperatures from – 40° Cto 125 ° C.

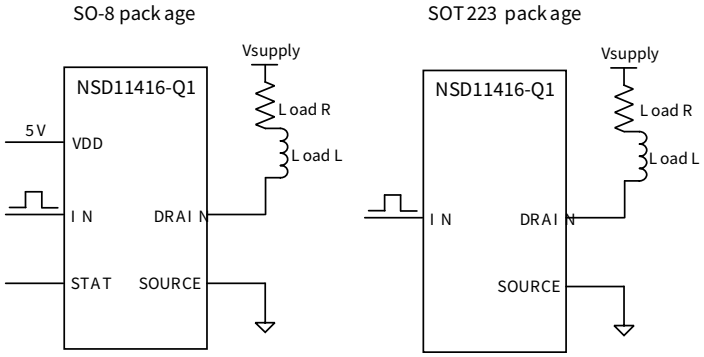
Key Features

- AEC-Q100 (Grade 1) q ualified for automotive applitio n
- Drain current limitation: 2.5 A
- 48V overvoltage clamp
- T hermal shutdown protection
- T hermal swing protection
- F ault diagnostic b lock
  - T hermal shutdown diagnosis
  - Short circuit to ground diagnosis
- Very low standby current
- Very low electromagnetic susceptib ility
- ESD protection
- RoHS & REA CH Compliance

App lcat ons

- Automotive Relays
- Valves
- Solenoid drivers
- L ighting

yp ca lApp lcat on



F igure 0.1 NSD11416-Q1 T ypical A pplication

Dev ce Infor at on

Part Nu ber	Pac age	Body ze
NSD11416-Q1SPR	SO-8	4.9 mm x 3 .9 mm
NSD11416-Q1ST BR	SOT 223	6.48mm x 3 .3 8mm

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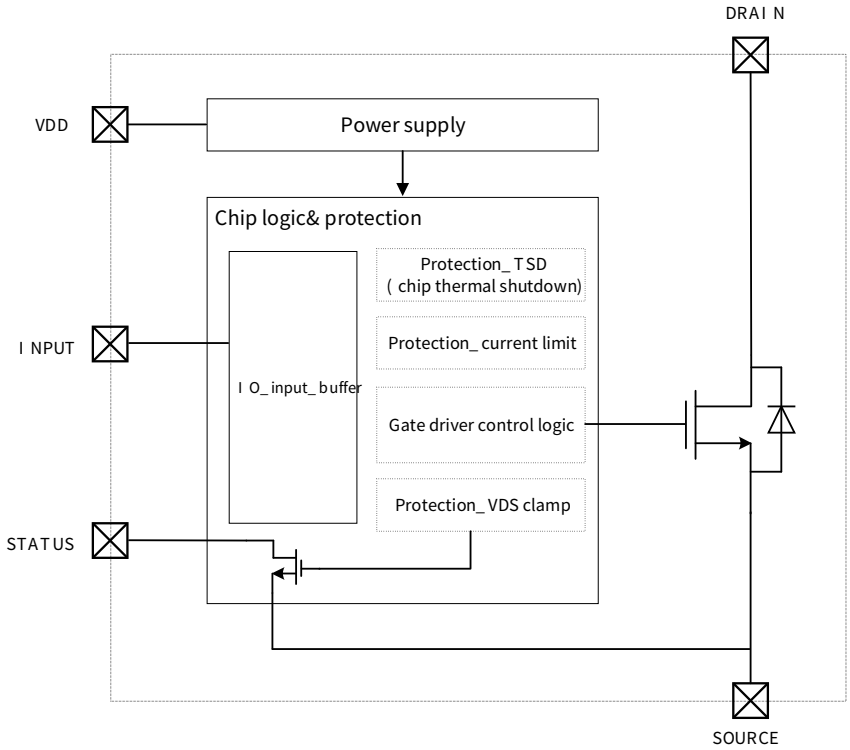
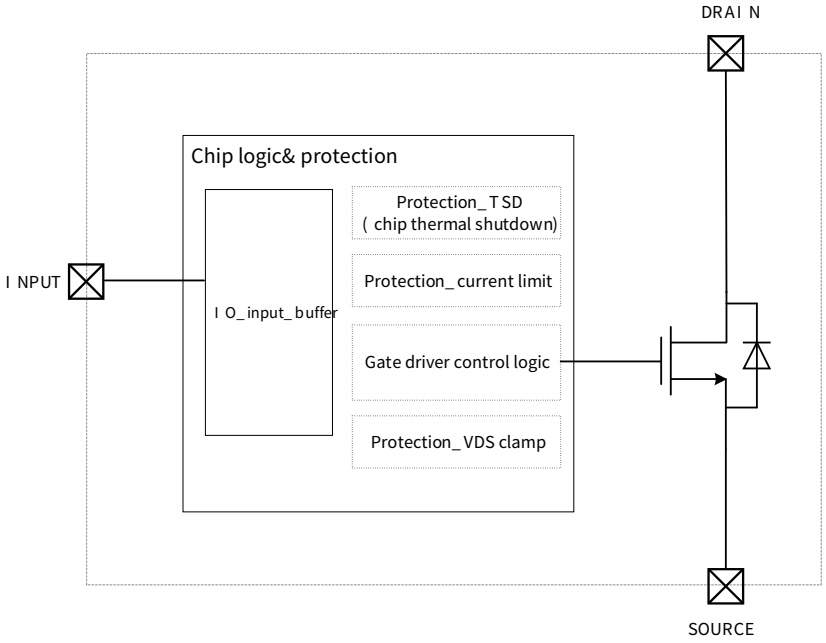


F igure 2.1 NSD11416-Q1SPR(SO-8) Block diagram



F igure 2.2 NSD11416- Q1ST BR (SOT 223) Block diagram

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Absolute Max u at ngs

Para eters	y bol	M n	yp	Max	u n t
Drain-to-Source Voltage	V_{DS}			I nternally clamped	V
DC Drain Current	I_D			Thermal limited	A
VDD Pin Current	I_{VDD}	-1		10	mA
I NPUT Pin Current	I_{IN}	-1		10	mA
STATUS Pin Current	I_{STAT}	-1		10	mA
J unction Temperature	T_J	-40		150	° C
Storage Temperature	T_{stg}	-55		150	° C
Single pulse avalanche energy (L = 30mH; T = 150 ° C; R 0; I_{OUT} = 2.2A)	E_{AS}			37	mJ

E D rat ngs

Para eters	y bol	a ue	u n t
V(ESD) Electrostatic discharge	Human-body model, per AEC-Q100-002-RevD， $V_{ESD-HBM}$	±4000	V
	Charged-device model, per AEC-Q100-011-RevB， $V_{ESD-CDM}$	±750	V

her a lInfor at on

Para eters	y bol	O	O	u n t
J unction-to-ambient Thermal Resistance	θ_{JA}	96.3	76.3	° C/ W
J unction-to-top characteriz ation parameter	ψ_{JT}	8.75	7.5	° C/ W
J unction-to-case (top) thermal resistance	$\theta_{JC(top)}$	49.3	46.9	° C/ W

The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, four layers board.

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pec f cat ons

E ectr ca lCharacter st cs

(V_{DD} = V_{IN} = 4.5 V to 5.5 V, T_J = -40° C to 150° C. Unless otherwise noted.)

Para eters	y bo l	M n	yp	Max	u n t	Co ents
Power MO FE						
Operating supply voltage	V_S	3.5	5	5.5	V	
ON-state resistance	R_{ON}		160		mΩ	I_D = 1 A; T_J = 25 ° C; V_{DD} = V_{IN} = 5 V
				320	mΩ	I_D = 1 A; T_J = 150° C; V_{DD} = V_{IN} = 5 V
Drain-source clamp voltage	V_{CLAMP}	46	48	56	V	V_{IN} = 0V, I_D = 1 A
Drain-source clamp threshold voltage	V_{CLTH}	40			V	V_{IN} = 0V, I_D = 2 mA
OFF-state output current	I_{DSS}	0		3	μA	V_{IN} = 0 V; V_{DS} = 13 V; T_J = 25 ° C
		0		5	μA	V_{IN} = 0 V; V_{DS} = 13 V; T_J = 125 ° C
Body diode forward voltage	V_{BD}		0.8		V	I_D = 1A; V_{IN} = 0 V
Input sect on O pac age on y						
Supply current from input pin	I_{ISS}		30	65	μA	ON-state: V_{DD} = V_{IN} = 5 V; V_{DS} = 0 V
Input clamp voltage	V_{CL}	5.5		8	V	I_S = 1 mA
			-0.7			I_S = -1 mA
Input threshold voltage	V_{NTH}	1		3.5	V	V_{DS} = V_{IN}, I_D = 1 mA
DD O pac age on y						
Operating supply current	I_S		10	25	μA	OFF-state; T_J = 25 ° C; V_{IN} = V_{DS} = 0 V;
			25	65	μA	ON-state; V_{IN} = 5 V; V_{DS} = 0 V
Supply clamp voltage	V_{SCL}	5.5		8	V	I_{SCL} = 1 mA
			-0.7			I_{SCL} = -1 mA
Log c Input O pac age on y						

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Para eters	y bo l	M n	yp	Max	ν n t	Co ents
High-level input current	$I_{I H}$			10	μA	$V_{I N}$= 2.2V
I nput hysteresis voltage	$V_{(hyst)}$	0.13			V	
I nput clamp voltage	V_{CL}	5 .5		8	V	$I_{I N}$= 1 mA
			-0.7			I_{N}= -1 mA
tatus nd cator O pac age on y						
Status low output voltage	V_{STAT}			0.5	V	I_{STAT}= 1 mA
Status leak age current	I_{STAT}			10	μA	V_{STAT}= 5 V
Status pin input capacitance	C_{STAT}			100	pF	V_{STAT}= 5 V
Status clamp voltage	$V_{ST CL}$	5 .5		8	V	I_{STAT}= 1 mA
			-0.7			I_{STAT}= - 1 mA
short c rcu t to ground detect on O pac age on y						
short circuit to ground OFF-state voltage detection threshold	V_{SCGTH}	1.1	1.2	1.4	V	$V_{I N}$= 0 V
Delay between I NPUT falling edge and STATUS falling edge in short circuit to ground condition	$t_{d (STAT)}$		225		μs	I_{OUT} = 0 A
w tch ng character st cs						
Turn-on delay time	$t_{d (ON)}$		9		μs	R_L = 13 Ω, V_{CC} = 13 V
Turn-off delay time	$t_{d (OFF)}$		9		μs	R_L = 13 Ω, V_{CC} = 13 V
Rise time	t_r		9		μs	R_L = 13 Ω, V_{CC} = 13 V
Fall time	t_f		5		μs	R_L = 13 Ω, V_{CC} = 13 V
Switching energy losses at turn-on	W_{ON}		26		μJ	R_L = 13 Ω, V_{CC} = 13 V
Switching energy losses at turn-off	W_{OFF}		23		μJ	R_L = 13 Ω, V_{CC} = 13 V
Protect on and d agnost cs						
DC short-circuit current	I_{lim}	1.6	2.5	3	A	V_{DS} = 13 V, V_{DD} = $V_{I N}$= 5 V
Shutdown temperature	T_{TSD}	150	175	200	° C	
Reset temperature	T_R	T_{RS} + 1	T_{RS} + 5		° C	
Thermal reset of STATUS	T_{RS}	135			° C	
Thermal hysteresis (T_{SD} - T_R)	T_{HYST}		7		° C	
Dynamic temperature	ΔT_J		40		° C	T_J = -40° C, V_{CC} = 13 V
Dynamic temperature hysteresis	$\Delta T_{J (HYS)}$		15		° C	

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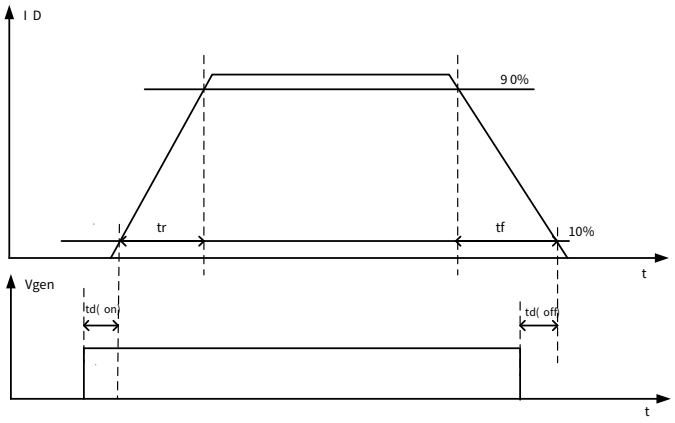
6.2. Typical Performance Characteristics

rue tab le

Conditions	*Input*	*Drain*	*Status*
Normal operation	L	H	H
	H	L	H
Current limitation	L	H	H
	H	X	H
Over-temperature limitation	L	H	H
	H	H	L
VDD under-voltage	L	H	X
	H	H	X
Short circuit to ground	L	L	L
	H	L	H

w tch ng character st cs



F igure 6.2.2 NSD11416-Q1 Switching Characteristics

Protect ons

Current L tat on

NSD11416-Q1 has current limitation to protect the silicon and bonding wire in case of overload or short circuit to battery.

her a lshutdown and ther a lsw ng

This device has both absolute and dynamic temperature protection. There are two thermal sensors on the controller and the MOSF ET, the one on the MOSF ET is the hottest and the one on the controller is the coldest. The absolute temperature protection is to shut down the MOSF ET when the hottest j unction temperature ex ceeds the T_{TSD}, and the dynamic temperature protection is also to shut down the MOSF ET when the temperature difference between the hottest and the coldest ex ceeds ΔT_J.

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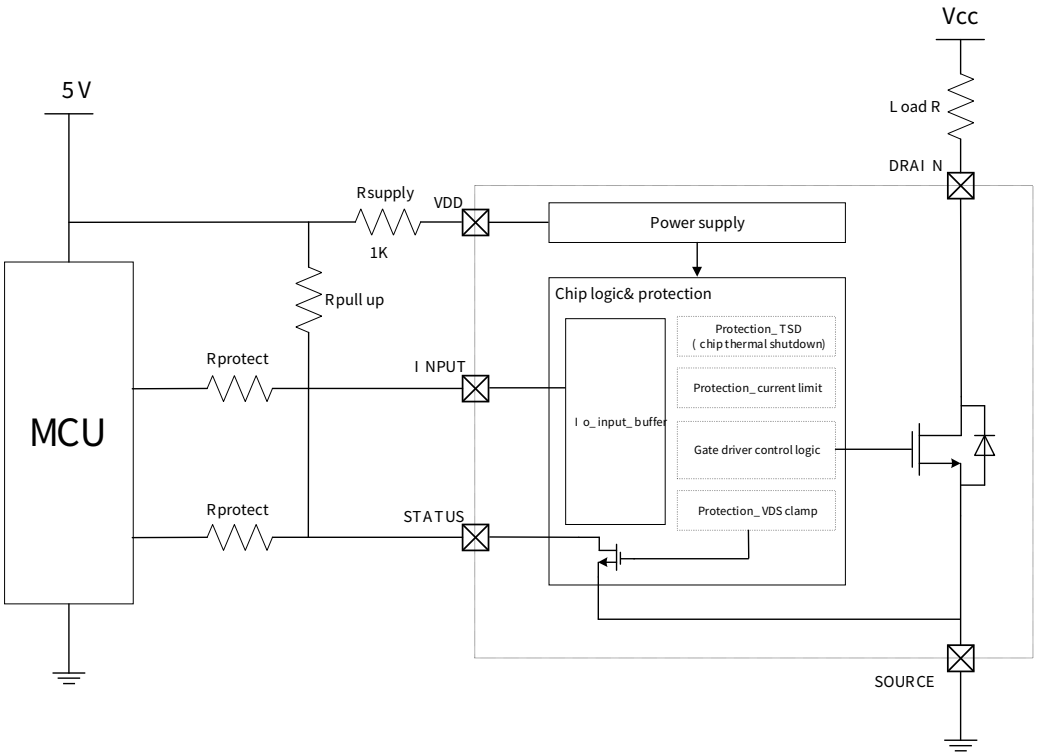
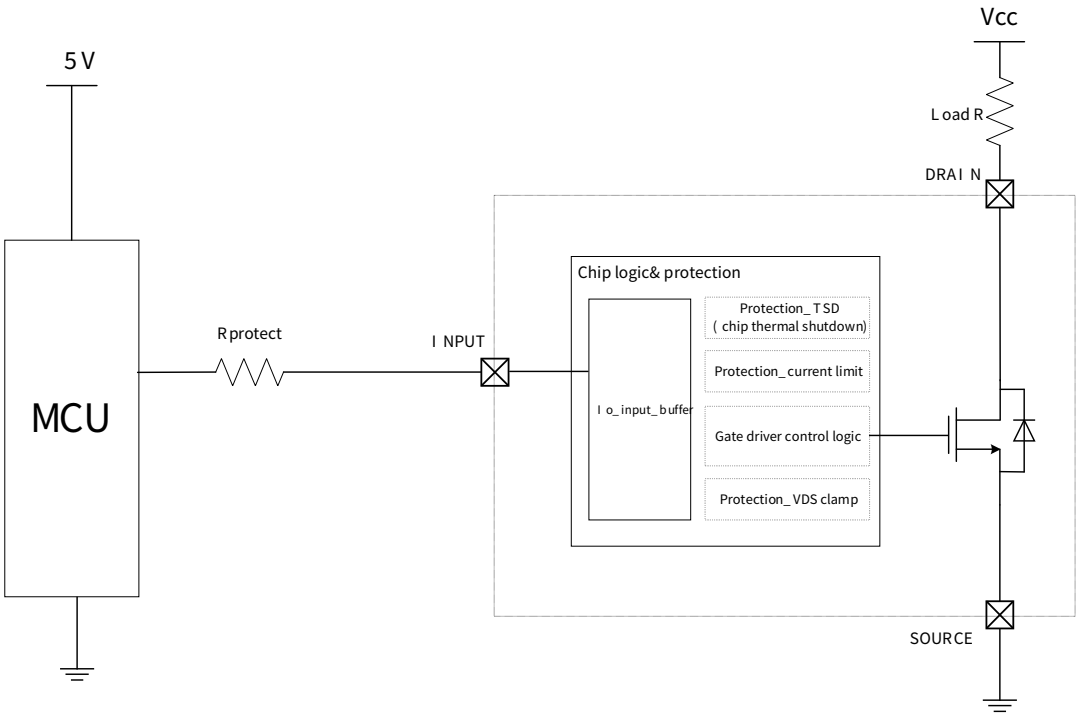
App lcat on nfor at on



F igure 8.1 NSD11416-Q1SPR application schematic



F igure 8.2 NSD11416-Q1ST BR application schematic

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MCU I O protection

NSD11416 has Zener diodes inside for ESD protection and the intrinsic NPN parasitic bipolar, so that resistors for protection are necessary in series with the digital inputs to limit the current to protect MCU I / Os during transient and reverse battery conditions.

The value of resistors for protection can be calculated by the formula as shown below:

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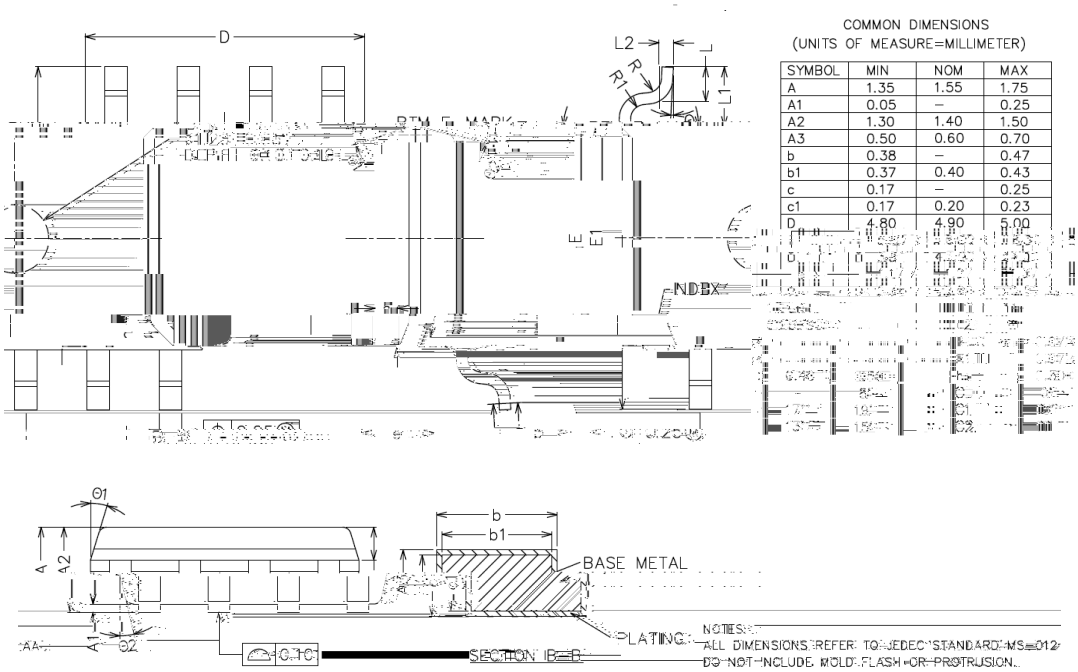
O pac_kage nfor at on



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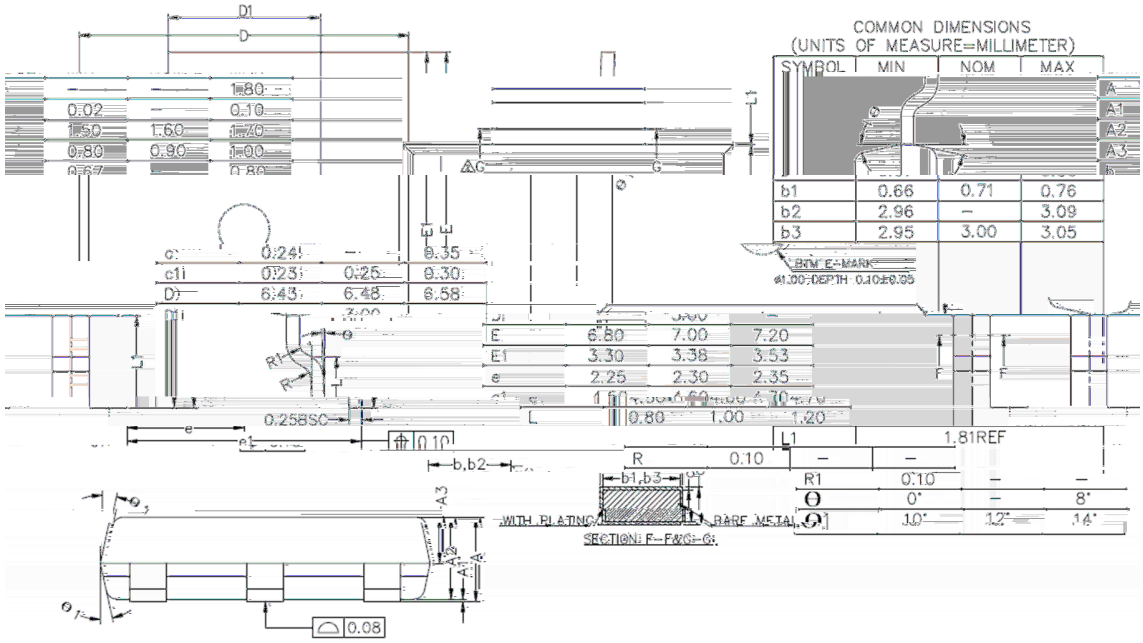

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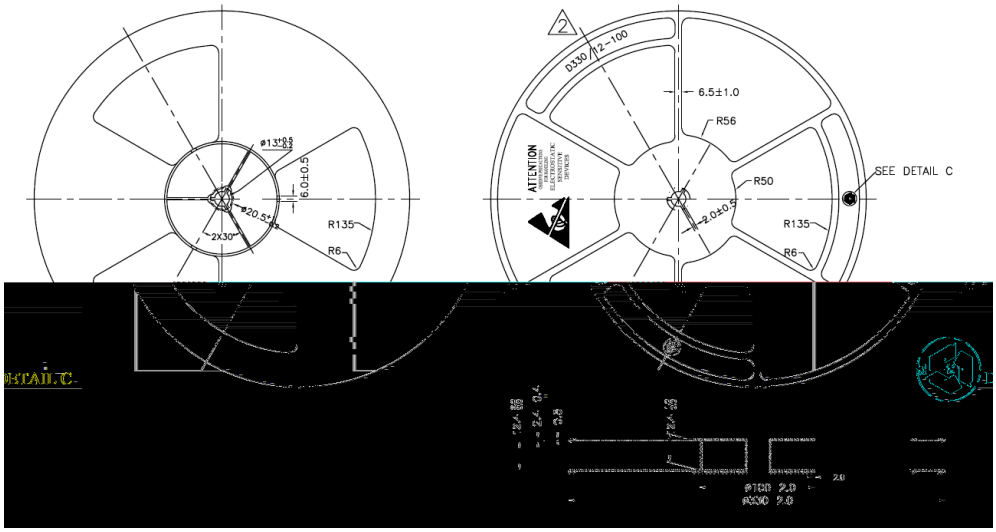
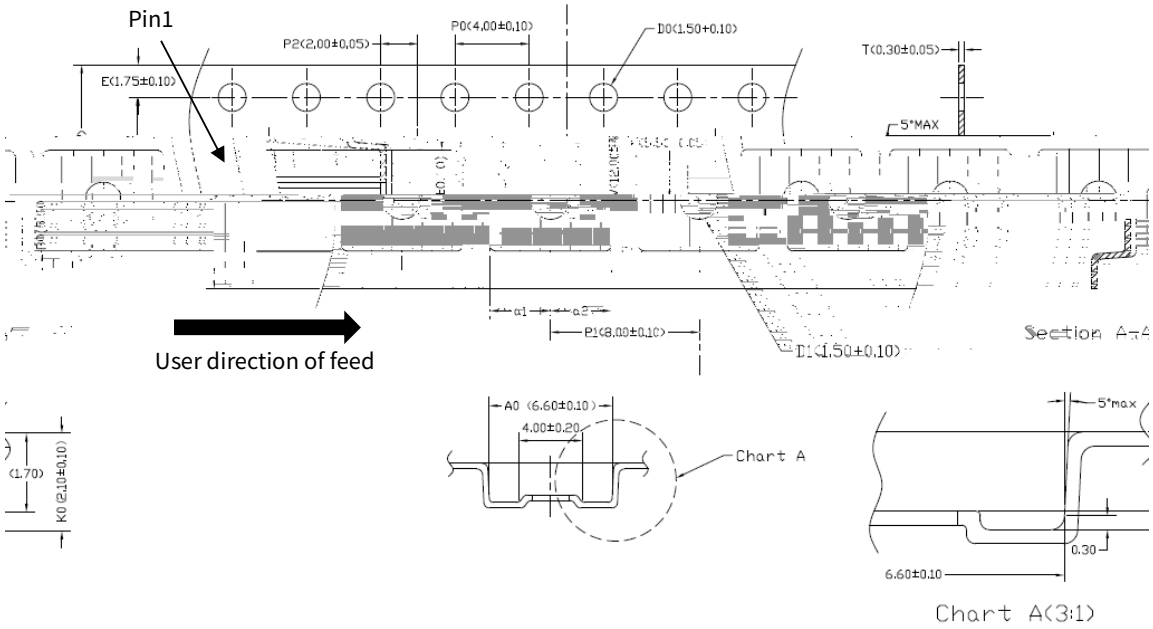
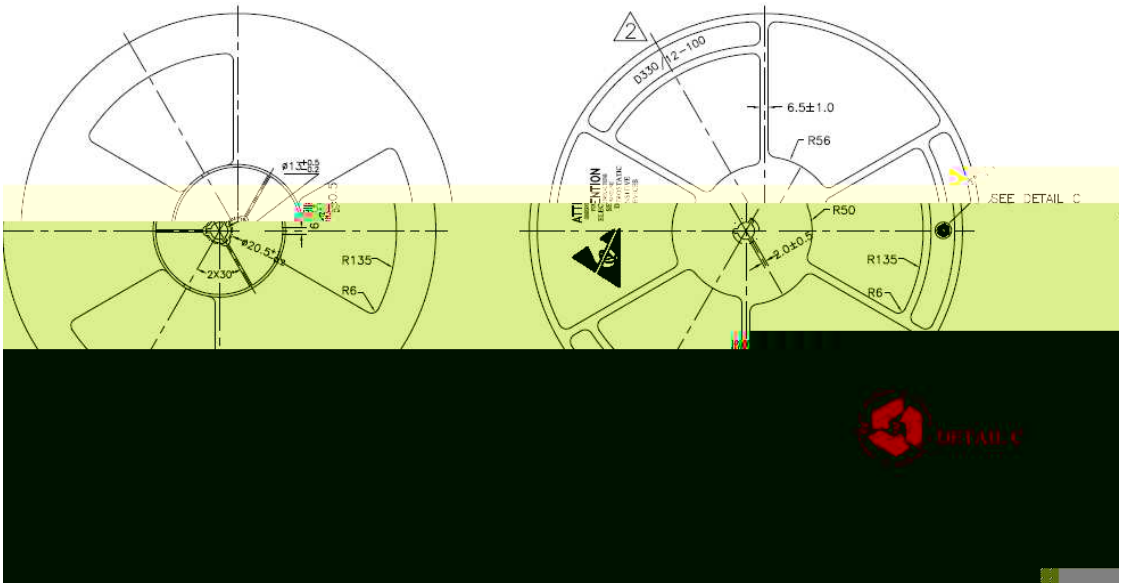
Pac ag ng Infor at on

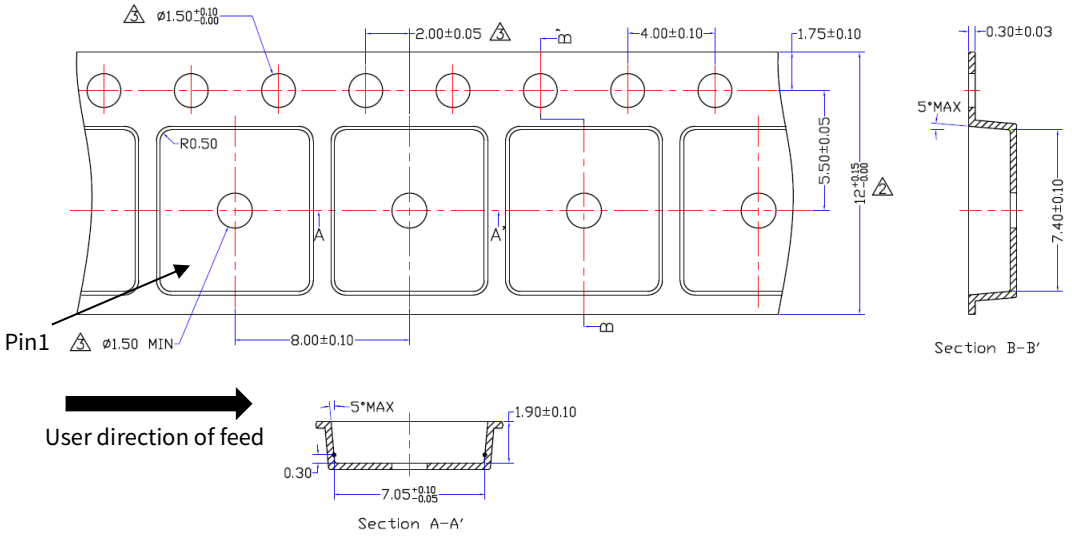
O pac ag ng nfor at on





10.2.SOT223 pac a!in! information





Order ng Infor at on

Part Nu ber	Pac age	M L	PQ
NSD11416-Q1SPR	SO-8	3	25 00
NSD11416-Q1ST BR	SOT 223	3	25 00
Note: All pack ages are ROHS compliant with peak reflow temperature of 260° C according to the J EDEC industry standard classifications and peak solder temperature.			

ev s on H story

ev s on	Descr pt on	Date
1.0	I nitial version	2024/ 1/ 3 1
1.1	Update description	2024/ 3 / 15
1.2	Update “ short circuit to ground OF F -state voltage detection threshold” max value	2024/ 4/ 7

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